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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
1035-473

Application Number	Filed
10/668,166	September 24, 2003
First Named Inventor: KIMURA	
Art Unit: 2811	Examiner: ARENA, Andrew O.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

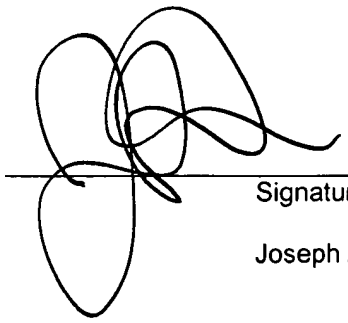
I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 37,515 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____



Signature

Joseph A. Rhoa

Typed or printed name

703-816-4043

Requester's telephone number

March 7, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KIMURA et al. Atty. Ref.: 1035-473; Confirmation No. 4031

Appl. No. 10/668,166 TC/A.U. 2811

Filed: September 24, 2003 Examiner: ARENA, Andrew O.

For: SEMICONDUCTOR DEVICE AND CHIP-STACK SEMICONDUCTOR DEVICE

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March 7, 2007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to the OG Notice of July 12, 2005, applicant hereby requests a pre-appeal brief review of this case for at least the following reasons.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Anderson in view of Hayasaka. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply, at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground, a particular signal-routing through electrode is formed of only one of the plurality of through electrodes; and at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip." In other words, at least one of the through electrodes "electrically link[s]" the front surface of the chip to the back surface of the chip and is a "*non-contact through electrode which is electrically isolated from the chip.*" For example and without

limitation, see the right-hand non-contact through electrode 19 in Fig. 3 of the instant application which is electrically isolated from the chip; and non-contact through electrodes 19 in Figs. 8-9.

The cited art fails to disclose or suggest the aforesaid underlined and quoted feature of claim 1. In particular, both Anderson and Hayasaka fail to disclose or suggest a non-contact through electrode electrically linking the front surface of the chip to the back surface of the chip which is a "*non-contact through electrode which is electrically isolated from the chip*" as required by claim 1.

The Office Action relies on Hayasaka at col. 11, lines 13-16, which states "not every chip having the metal plugs 4 need be connected with its neighbor by means of the plugs . . . that is, one or more of the chips may be formed with metal plugs only for the purpose of heat radiation." First, it is pointed out that this portion of Hayasaka only appears to describe that the chip is not connected with its neighbor via the metal plug. Therefore, this relates to the connection between a metal plug in one chip and another metal plug in the chip above or below. This portion of Hayasaka does not describe a non-contact through electrode that is electrically isolated from the chip.

The Office Action appears to argue that, based on Figs. 4-5, and col. 10, lines 20-25, of Hayasaka, that the metal plug is isolated from the chip portions surrounding the plug. However, claim 1 requires that the non-contact through electrode is electrically *isolated from the* ***chip***. Claim 1 does not recite "chip portions surrounding the plug." The metal plugs relied on by the Office action in Figs. 4-5 of Hayasaka are clearly in electrical contact with the chips through which they pass, as evidenced by col. 10, lines 35-40, which describes that the metal plugs 4 electrically connect through solder bumps . . . allowing the chips 1b and 1c to be connected. Moreover, Fig. 8 also shows that the plug is in electrical communication with the chip. Thus, the metal plugs relied on by the Office Action to allegedly support the position that the metal plugs are electrically isolated from the chip are indeed *not* electrically isolated from the chips. Hayasaka teaches directly away from the invention of claim 1 in this respect.

Accordingly, even the alleged combination of Anderson and Hayasaka (which applicant believes would be incorrect in any event) fails to disclose or suggest (1) a through electrode which *electrically links* the front surface of a chip to a back surface of a chip, *and* (2) the *same*

through electrode is *electrically isolated* from the chip in which it is formed. Thus, the cited art fails to disclose or suggest the subject matter of claim 1.

The Examiner alleges in the 2/6/07 Advisory Action that "Hayasaka teaches at col. 11, lines 13-17 that at least some electrodes are formed in their host chip 'only for the purpose of heat radiation' which directly suggests that there is no desire for those electrodes to provide electrical contact to that host chip." However, this citation in the Examiner's argument only states that not every chip is connected with its neighbor by means of metal plugs. The metal plugs in Figs. 4 and 5 of Hayasaka are clearly in electrical contact with the chips through which the metal plugs pass. Therefore, the metal plugs in Hayasaka are not electrically isolated from the chip – this is the opposite of what claim 1 requires.

The Examiner in the Advisory Action also relies on the MPEP. However, the references cited in §2144.04 II taught that particular salts were not beneficial when they were not employed in a fresh water environment and therefore the salts could be omitted at that time. However, Hayasaka and Anderson do no have provisos as seen in the legal precedent (in the case of Hayasaka, Hayasaka does not have an explanation as to when there is no desire for the electrodes in Hayasaka to provide electrical contact to the host chip). Thus, there is no suggestion in the cited art to omit any element. The Advisory Action's reliance on §2144.04 is misplaced.

The Examiner in the Advisory Action also contends that although the plugs' only purpose in the chip is to carry heat, they may additionally serve the purpose of carrying electricity through that chip between other chips. However, metal plugs of Hayasaka that are formed only for the purpose of heat radiation do not carry an electrical current. The metal plugs are formed only for heat radiation and so they are not intended to carry an electrical current (in contrast, many plugs in claim 1 carry current, e.g., see the first high-current through electrode in claim 1). Although it may be possible to cause the metal plugs to carry an electrical current, Hayasaka neither teaches nor intends causing the metal plugs formed only for heat radiation to carry an electrical current. There is no reason for causing the metal plugs formed only for heat radiation to carry an electrical current. Thus, Hayasaka's statement of using plugs only for the purpose of heat radiation in col. 11 teaches directly away from claim 1's requirement of multiple through electrodes connected to each other to form a high current through electrode – one of ordinary

skill in the art would never have used Hayasaka's plugs in this respect. Moreover, if this feature of claim 1 was omitted as suggested by the Examiner, the claim would not be met.

The Examiner contends in the Advisory Action that it would have been obvious to connect plural through electrodes to provide GND and VDD at a lower impedance than using single electrodes. This motivation for the alleged Section 103(a) modification lacks merit and is clearly erroneous. Anderson teaches connecting plural solder bumps in order to provide GND and VDD in various parts of the chips, and the connection of plural solder bumps in Anderson is totally unrelated to reducing impedance. This is because impedance is already reduced in Anderson by using wide, thick wires. Because impedance is already reduced in Anderson, there is no such motivation for the alleged combination of Anderson with Hayasaka.

Claim 7 requires that "at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed." Moreover, claim 8 requires that "at least one of the through electrodes is a non-contact through electrode which is electrically isolated from the semiconductor chip in which it is formed." The cited art fails to disclose or suggest each of these features of claims 7 and 8, respectively.

Regarding claims 9, 11, 12, 13, 15-17, 19 and 20, the Office Action has used impermissible hindsight reasoning to arrive at the claimed inventions. The Office Action asserts that it is well known that a larger total cross section is used for a longer conduction path to reduce impedance. The Office Action then asserts that one skilled in the art would connect through electrodes in order to reduce impedance. This latter assertion is certainly based on impermissible hindsight reasoning. Anderson teaches reducing impedance by using a wide, thick wire at col. 3, lines 57-64. Assuming arguendo for the sake of argument only that one were to combine Anderson and Hayasaka, one skilled in the art wishing to reduce impedance would apply the teaching of Anderson and provide wider, thicker metal plugs. However, the pending claims call for through electrodes with substantially equal cross-sectional area, so this modification would not meet the pending claims. Moreover, Anderson teaches connecting a plurality of solder bumps in order to provide GND and VDD to various parts of the chips, the connection of multiple solder bumps in Anderson is entirely unrelated to reducing impedance; impedance is reduced in Anderson by using wide, thick wires. Thus, the rationale alleged by the Examiner for the combination lacks merit and is fundamentally flawed. Stated another way, one

of ordinary skill in the art would not have made the modification alleged at page 7, lines 7-14, in order to reduce impedance as alleged by the Office Action; instead, one would have reduced impedance by using wide, thick wires as taught by Anderson.

It is respectfully requested that all rejections be withdrawn.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

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